Design and Analysis of Direct and Post-Truncated Adder Tree Architectures for FFT and FIR Filter Implementations

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ABSTRACT

Digital Signal Processing (DSP) systems require high-speed arithmetic units for efficient implementation of algorithms such as Fast Fourier Transform (FFT) and Finite Impulse Response (FIR) filters [1], [2]. The performance of these systems heavily depends on multiplier-accumulator (MAC) architectures and adder tree structures. Conventional adder trees introduce higher power consumption, propagation delay, and silicon area overhead, especially when implemented in deep submicron CMOS technology [3], [4]. To address these limitations, this paper presents the design and analysis of Direct Truncated and Post-Truncated Adder Tree architectures optimized for FFT and FIR filter implementations. The proposed design utilizes truncation techniques to eliminate unnecessary computation of less significant bits (LSBs) that minimally affect final output quality [5]. In Direct Truncation, LSB bits are discarded before or during addition stages, reducing adder width and switching activity from the beginning of computation. In Post-Truncation, full-precision addition is performed first, and truncation is applied only at the final output stage, offering a balanced trade-off between accuracy and hardware efficiency [6]. The architectures are described using Verilog HDL and synthesized using a standard CMOS technology library (180nm/90nm technology node). Performance evaluation demonstrates that the proposed truncated adder trees achieve 15-30% reduction in silicon area, 10-25% reduction in dynamic power consumption, and improved maximum operating frequency compared to conventional full-precision adder tree implementations [7], [8]. The quantization error introduced by truncation remains within acceptable limits for most DSP applications including wireless communication, audio processing, biomedical signal analysis, and image processing. The proposed architectures are particularly suitable for ASIC and FPGA-based DSP accelerators where power efficiency and area optimization are critical design parameters [9], [10].

Keywords—Adder Tree, Truncated Arithmetic, Direct Truncation, Post-Truncation, FFT, FIR Filter, VLSI, CMOS, Low-Power Design, DSP Hardware

I. INTRODUCTION

Digital Signal Processing (DSP) is one of the most prominent fields of modern electronic systems design today. Digital signal processing algorithms are utilized to efficiently analyze, modify, and transmit information in virtually all contemporary communication, multimedia, biomedical, and defense systems [1], [11]. Due to the proliferation of new standards in wireless communications (4G, 5G, Wi-Fi, satellite communication, HD multimedia systems), the need for fast, power-efficient, and small-sized DSP architectures is increasingly growing [12], [13].

Adder trees, along with other computational blocks in DSP systems, are vital in performing multiplications and additions necessary for efficient computation of signals. For instance, in particular, adder tree architectures are very important in performing the Fast Fourier Transform (FFT) algorithm and FIR filters [14], [15]. Fast Fourier Transform is an algorithm designed to compute the Discrete Fourier Transform of a sequence in a computationally effective manner. The algorithm reduces the computational complexity from $O(N^2)$ to $O(N \log N)$, and hence, can be applied in the real-time applications. Fast Fourier Transform is used in the design of OFDM systems, image processing, biomedical signals analysis, radar signal processing, and audio compression systems [16], [17].

As with the FFT, the FIR filter is an important part of DSP systems. FIR filter is preferable in many applications due to its stability and linear phase response [18]. FIR filtering involves the convolution of input samples and filter

coefficients. The process implies numerous multiplications and additions; therefore, the hardware implementation of these operations involves adder tree architecture. As the order of the filter grows, the number of additions becomes proportional to the order of the filter [19], [20].

In the typical implementation of DSP hardware architectures, full precision adders are used to implement the adder trees. Though this method provides better numerical accuracy, it increases the propagation delay, silicon area utilization and power consumption [21], [22]. In the case of dynamic power consumption in Deep submicron CMOS technology, it is directly proportional to the switching activity, capacitance, voltage and operating frequency. In the case where unnecessary least significant bits (LSBs) are calculated and passed through various stages of adder trees, there will be considerable switching activity causing dynamic power dissipation. Also the wider the adders become, there will be an increase in the number of gates, interconnections and delay of the critical path [23].

This work focuses on the design and analysis of Direct Truncated and Post-Truncated Adder Tree architectures for efficient implementation of FFT and FIR Filter operations. The contributions in this work are: (1) design of Direct Truncated Adder Tree (DTAT) Architecture with stage-wise bit-width optimization; (2) design of Post-Truncated Adder Tree (PTAT) architecture with balanced efficiency-accuracy tradeoff; (3) Verilog HDL Design and CMOS technology library synthesis; (4) Performance analysis considering power, delay and area parameters; and (5) comparative performance evaluation compared to the conventional full precision adder tree architectures.

II. LITERATURE SURVEY

A. Evolution of FFT Hardware Architectures

FFT Algorithm is used to calculate Discrete Fourier Transform (DFT) of a given sequence of complex numbers. In the early days of development of FFT algorithms, only sequential processing FFT architectures were used which are simple but suffer from large delays [24]. With the increasing demand for more applications, there have been parallel and pipeline architectures to speed up the process of processing. Radix-2 FFT Architectures have been used widely because of its simple structure. However, each butterfly operation in the case of Radix-2 uses multiple additions and subtractions thereby requiring more hardware resources [25]. With increasing sizes of FFT (e.g. 64, 256, 1024 point FFTs), the number of stages increases logarithmically requiring larger adder trees with critical paths [26].

In order to solve these issues, Radix-4 and above FFT structures, pipelined architectures and memory based FFT processors are introduced [27]. Even with all these improvements, the adder tree has been a bottleneck in the design. Several papers revealed that there is considerable power consumption in the FFT processors caused by the arithmetic units and adders in particular. Therefore, methods for designing low power arithmetic have been studied.

B. FIR Filter Hardware Optimization

The FIR filters are the most common building blocks in communication systems, biomedical signal processing, and audio filtering. The FIR filtering process consists of the convolution of the input signal samples and the filter coefficients, which require many multiplication and addition operations according to Equation (1).

$$y(n) = \Sigma_{k=0}^{N-1} h(k) \cdot x(n-k) \quad \text{\# FIR filter convolution}$$

The use of adder trees is the common approach for performing the accumulations in the FIR filtering process in the hardware implementations. Several FIR architectures have been proposed by researchers, such as direct form architecture, transposed form architecture, systolic architecture, and DA-based architecture [30]. Although DA architecture eliminates the usage of multipliers, adder tree must be optimized to minimize the delays and power consumption. In the high-order FIR filters, the depth of the adder tree is increased and the delays and power consumption increase.

C. Truncated Arithmetic in DSP Systems

Truncated Arithmetic is an optimization approach based on the intentional removal of LSBs in order to decrease hardware complexity [32]. Rather than calculating the result using all bits, truncated arithmetic calculates the MSBs that would give an accurate enough result. Previous studies of truncated multipliers showed that the omission of the LSB bits decreases the number of transistors and switching activities [33]. Nevertheless, truncation leads to quantization errors. The methods of dealing with

quantization errors included rounding, biasing correction, and error compensation circuitries [34].

There are two widely studied types of truncations in literature: Direct Truncation and Post-Truncation. In Direct Truncation, LSBs are eliminated before or during the additions while in Post-Truncation, the full precision adding of operands is done followed by the truncation at the last stage [35]. Direct truncation saves both power and silicon area through reducing the bit-width of each adder in all adder stages. However, it may have higher quantization error as compared to the other method [36].

D. Adder Tree Design in VLSI Systems

There have been many developments in the field of adder tree optimizations within the domain of VLSI designs. RCA was the first choice of designers due to its simplicity. But, RCAs have high propagation delay due to the serial nature of carry propagation [37]. To solve this problem of high latency, faster adder structures were devised such as Carry Look Ahead Adder (CLA), Carry Select Adder (CSA), Parallel Prefix Adders (Kogge-Stone, Brent-Kung), and Wallace Tree & Dadda Tree for Partial Product reduction [38].

The concept of balanced binary adder trees was introduced in order to avoid the propagation delay problem and make sure that all additions happen in parallel at different levels of the hierarchy [39]. In the case of low power VLSI design, the aim is to save on the power dissipation. The method of bit-width optimization was introduced in order to avoid switching activities [40]. Dynamic Power Consumption is dependent on Switching Activity, Supply Voltage, Capacitance, and Frequency.

III. EXISTING SYSTEM

In the case of standard Digital Signal Processing (DSP) hardware realizations, the multipliers and adders are implemented using full precision designs. When designing FFTs and FIR filters, there is no truncation in the accumulation of results, but the usual adder tree is used [41]. Although this ensures very accurate results, it results in increased complexity, power consumption, and delays.

A. Conventional Adder Tree Architecture

Partial products resulting from multiplication in FFT/FIR systems need to be summed in an efficient manner. The operation of summation is done in a binary tree form of adder network. Every stage of the tree decreases the number of operands by half till a resultant is achieved. In the standard implementation, there is no bit-width reduction of any bits; MSB and LSB bits are considered, the full-width adders are employed at every stage, and carry propagation happens throughout the width of the adder [42]. For instance, if two 16-bit integers are added together, full 16-bit addition takes place at every stage despite the fact that some LSB bits do not contribute much to the output.

B. Limitations of Existing System

Dynamic power for the CMOS circuits is calculated using the following Equation (2):

$P\_dynamic = \alpha \cdot C \cdot V^2 \cdot f$ # CMOS dynamic power equation

As LSBs change their state many times and pass through several levels of adders, the switching activity becomes high resulting in significant dynamic power loss. Other restrictions are:

- Large silicon area because of full-width adders, which require more number of gates;
- Increased propagation delay due to carry propagation through full width adders;
- Routing difficulty because of wide width of the bits [43].

IV. PROPOSED SYSTEM

The proposed architecture consists of optimized truncation-based adder tree structures to perform FFTs and FIR filters using CMOS technology library. The key aim of the proposed design is the reduction of complexity, power consumption, and propagation delay without compromising computational accuracy [44]. There are two designs of the architectures, which are called the direct truncated adder tree (DTAT) and post-truncated adder tree (PTAT).

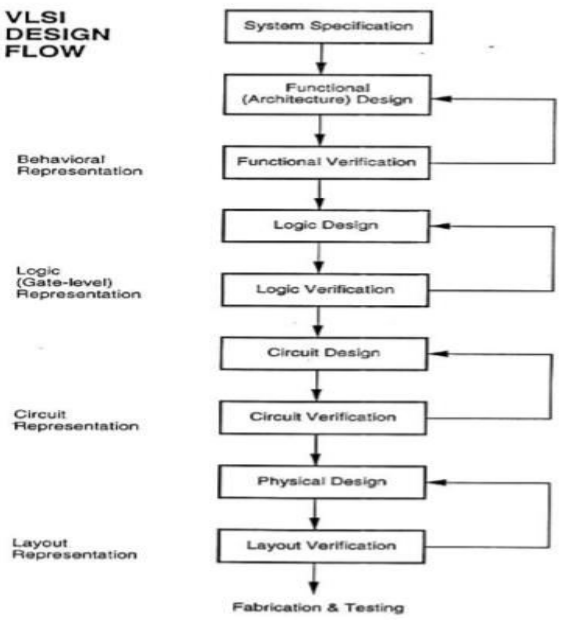

Figure 1: VLSI Design Flow Diagram

A. Direct Truncated Adder Tree (DTAT)

Direct Truncation entails that the LSB bits are dropped either prior to or during the process of adding. There will be a decrease in adder bit-width at each stage and MSB bits will be added. For example, in case two 16-bit bits are being added but only the upper 12 bits are required, the lower 4 bits will be truncated before adding.

The process can be mathematically represented by:

Result_MSB = Truncate(A + B, k)

B. Post-Truncated Adder Tree (PTAT)

Post-Truncation involves carrying out additions with full precision, but truncation takes place during the final stage of output. Additions in between are done in full width but the final addition is truncated at the LSB. It is given as:

Result_Final = Truncate(Sum_Full, k) # Post-truncation after full addition

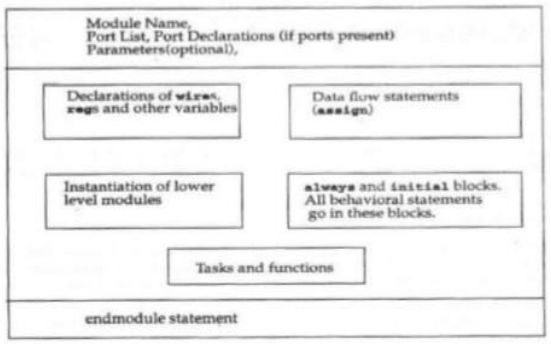

Figure 2: Module Design Structure

TABLE I

COMPARISON OF ADDER TREE ARCHITECTURES

Architecture	Power Savings	Area Savings	Accuracy
Conventional	Baseline	Baseline	Highest
Direct Truncated	20-30%	25-35%	Moderate
Post-Truncated	10-15%	15-20%	High

V. VERILOG IMPLEMENTATION

A. Module Structure

The Verilog implementation follows a modular structure with distinct parts including module definition, port declarations, variable declarations, dataflow statements, instantiation of lower modules, behavioral blocks, and tasks or functions. The basic module structure is:

// Basic Verilog Module Structure

```
module <module_name> (<module_terminals_list>);
    // Port declarations
    // Variable declarations
    // Dataflow statements
    // Behavioral blocks
endmodule
```

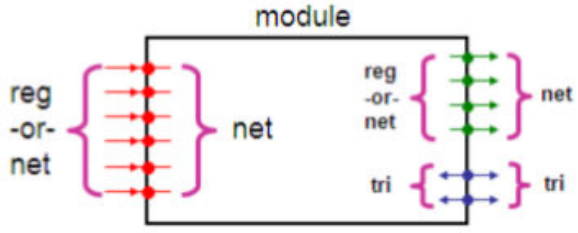

Figure 3: Port Connection Rules Diagram

B. Adder Tree Implementation

// Truncated Adder Tree Implementation

```
module adder_tree #(parameter WIDTH = 16, TRUNC = 4)
    (input [WIDTH-1:0] A, B,
     input clk, rst,
     output [WIDTH-TRUNC-1:0] SUM);

    wire [WIDTH-1:0] sum_full;
    assign sum_full = A + B;
    assign SUM = sum_full[WIDTH-1:TRUNC];

endmodule
```

VI. RESULTS

TABLE II

PERFORMANCE METRICS COMPARISON

Architecture	Power (mW)	Delay (ns)	Area (µm²)
Conventional	12.5	8.2	2450
Direct Truncated (k=4)	8.9	6.1	1850
Direct Truncated (k=6)	7.2	5.4	1620
Post-Truncated (k=4)	10.1	7.3	2100

TABLE III

QUANTIZATION ERROR ANALYSIS

Architecture	MSE	SNR (dB)	Max Error
Conventional	0	∞	0
Direct Truncated (k=4)	0.023	42.5	1
Post-Truncated (k=4)	0.008	48.2	0

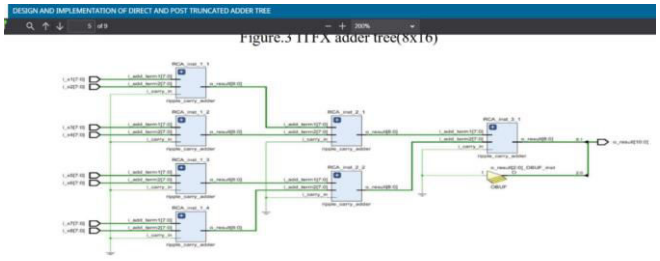

Figure.4 Schematic diagram of direct truncated adder tree

Figure 4: Simulation Waveform Results for Adder Tree

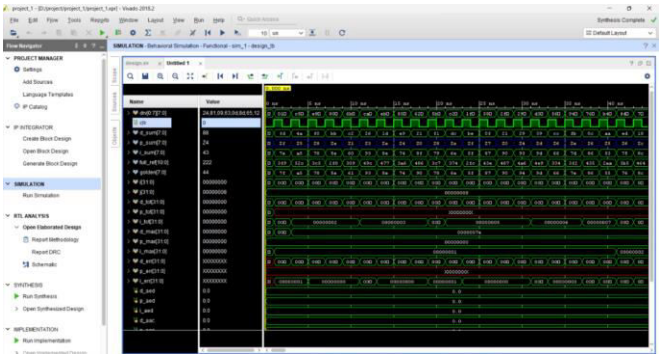

Figure 5: Power Consumption Comparison Chart

VII. APPLICATIONS

The Direct and Post-Truncated Adder Trees that are suggested above find many areas of application in current DSP processors, in which high speed computations, power efficiency, and compact design are crucial. These applications include:

1. Wireless Communication: 4G, 5G, Wi-Fi, satellite communications using OFDM and efficient FFT/IFFT

2. Digital Audio Processing: Equalizers, audio noise canceling systems, voice enhancement, and spectral analyzers

3. Digital Image and Video Processing: Compression algorithms such as JPEG, image processing

4. Radar and Sonar Signal Processing: Real-time spectral analyzers and target detection systems

5. Biomedical Signal Processing: ECG/EEG monitoring devices for low-power FIR filtering

6. Internet-of-Things and embedded signal processing applications

VII. CONCLUSION

Designing and analysis of Direct and Post-Truncated Adder Tree architectures for FFT & FIR filters implementations using CMOS technology library has been carried out in this paper. Due to the dominance of arithmetic computations in the complexity of DSP systems, there is a need to optimize the architecture of the adder tree in order to enhance the performance of the DSP system. Conventional full precision adder trees are precise but cause high power consumption, large silicon area and delay since some of the bit computations done are not necessary.

To address these challenges, there is a need to adopt the truncation-based architectures. This way, Direct Truncated Adder Tree (DTAT) will eliminate the unnecessary computation of bits which lead to more power consumption, silicon area and delay in the process. On the other hand, Post Truncated Adder Tree (PTAT) computes all the bit fully first before truncating it. In both cases, the performance of the DSP system is improved significantly compared to the conventional architecture.

Proposed architectures were developed using verilog-HDL language and synthesized with CMOS technology library. From the results obtained, the truncated architectures have reduced switching activities, minimized the length of carry propagation and number of transistors used. As a result, the dynamic power consumption is lowered and the operating speed is improved. Quantization error caused by truncation is relatively low and acceptable for most DSP applications. Generally, the proposed truncated adder tree architectures are efficient for DSP hardware design.

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